UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/762,277	01/23/2004	Shinichi Kurose	1614.1381	4700

21171 7590 06/03/2005

STAAS & HALSEY LLP
SUITE 700
1201 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005

EXAMINER	
TAT, BINH C	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 06/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H'A

Office Action Summary	Application No.	Applicant(s)	
	10/762,277	KUROSE ET AL.	
	Examiner	Art Unit	
	Binh C. Tat	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *01/23/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application 10/762277 file on 01/23/04.

Claim 1-16 remain pending in the application.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-16 are rejected under 35 U.S.C. 102(b) as being anticipated by Takenaka et al. (US Patent 5699289).

3. As to claims 1, and 8, Takenaka teaches a semiconductor integrated circuit, comprising: a block having a first border edge on which an external connection terminal provided and second border edge on which no external connection terminal is provided (see fig 2, 3, 4 and 9 col. 3 lines 50 to col. 4 lines 15); a wiring prohibited area (see fig 4 and 9 element 48) which extends a first distance from the first border edge and in which no wiring line running parallel to the first border edge exists (see fig 2-4 and 9 col 4 lines 15-52); and a shielding line which is at second distance from the second border edge and runs parallel to the second border edge (see fig 2-4 and col. 3 lines 65 to col 4 lines 52 and col 7 lines 31-43).

4. As to claims 2, Takenaka teaches wherein said block is completely enclosed by border edges that are either the first border edge or the second border edge (see fig 1 2, and 4 element 40, PSLC and PSLR).

5. As to claims 3, Takenaka teaches wherein said wiring prohibited area is situated inside the first border edge, and said shielding line is situated inside the second border edge (see fig 4 and 9 element 48).

6. As to claims 4, Takenaka teaches wherein said wiring prohibited area is situated outside the first border edge, and said shielding line is situated outside the second border edge (see fig 4 and 9 element 48 and col 4 lines 32-52).

7. As to claims 5, Takenaka teaches wherein said wiring prohibited area is situated inside and outside the first border edge, and said shielding line is situated inside and outside the second border edge (see fig 4 and 9 element 48 and col 4 lines 32-52).

8. As to claims 6, Takenaka teaches wherein said block is a physical block that is a layout area divided on a function- by-function basis in hierarchical layout designing (see fig 16-20).

9. As to claims 7, Takenaka teaches wherein the first and second border edges, the wiring prohibited area, and the shielding line are provided in a first wiring layer, and said block has third border edge which an external c6nnection terminal is provided and fourth border edge on which no external connection terminal is provided, the third and fourth border edges being provided a second wiring layer that is different from the first wiring layer, said semiconductor integrated circuit further comprising: a wiring prohibited area which extends a third distance from the third border edge and in which no wiring line running parallel to the third border edge exists (see fig 3 col 4 lines 15-31); and a shielding line which is at a fourth distance from the fourth border edge and runs parallel to the fourth border edge (see fig 2-3 col 3 lines 65 to col 4 lines 31).

10. As to claims 9, Takenaka teaches further comprising a step of cutting out a physical block as said block area, said physical block being a layout area divided on a function-by-function basis at a top level in hierarchical layout designing (see fig 16-20).

11. As to claims 10, Takenaka teaches wherein said steps through c) are repeated with respect to each wiring layer (see fig 3 and fig 4 col 4 lines 15-52).

12. As to claims 11, Takenaka teaches wherein the first distance is longer than a minimum wiring distance (see fig 3 and fig 4 col 4 lines 15-52).

13. As to claims 12, Takenaka teaches wherein the second distance is equal to a minimum wiring distance (see fig 3 and fig 4 col 4 lines 15-52).

14. As to claims 13, Takenaka teaches wherein the third distance is longer than a minimum wiring distance (see fig 3 and fig 4 col 4 lines 15-52).

15. As to claims 14, Takenaka teaches wherein the fourth distance equal to a minimum wiring distance (see fig 3 and fig 4 col 4 lines 15-52).

16. As to claims 15, Takenaka teaches wherein the first distance is longer than minimum wiring distance (see fig 3 and fig 4 col 4 lines 15-52).

17. As to claims 16, Takenaka teaches wherein the second distance is equal minimum wiring distance (see fig 3 and fig 4 col 4 lines 15-52).

Conclusion

18. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Binh C. Tat whose telephone number is (571) 272-1908. The examiner can normally be reached on 7:30 - 4:00 (M-F).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mathew Smith can be reached on (571) 272-1907. The fax phone numbers for the organization where this application or proceeding is assigned are (571) 273-1908 for regular communications and (703) 305-3431 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-1782.

Binh Tat
Art unit 2825
January 21, 2005

THUAN DO
Primary examiner
05/28/2005